REMARKS/ARGUMENTS

Claims 1-10, 12-19, and 21-28 are pending in the present patent application. Claims 1-2, 5, 7, 10, 12-13, and 17 have been amended. No new matter has been added to the amended claims. Claims 11, 20, and 29 were canceled in a previous amendment. Reconsideration of the claims is respectfully requested.

A request for continued examination (RCE) is being filed herewith.

Allowable Subject Matter

The office action allowed claims 21-28. The office action also indicated that claims 2-4, 6, 8-10, and 13-19 contain allowable subject matter. Claims 2, 10, and 13 have been amended into independent claims.

Prior Art Rejections of Claims 1 and 12

The office action rejected claims 1, 7, and 12 as being anticipated by U.S. Patent 5,905,291 to Utsunomiya et al.

Claims 1 and 12 have been amended to address these rejections. Claim 1, for example, has been amended to recite "a first native transistor with a threshold voltage that is greater than zero over a voltage range caused by process variations."

The Utsunomiya et al. patent discloses that "MOSFETs M0 through M14 utilize MOSFETs of an enhancement type wherein the threshold value is proximate to 0 V (approximately 0.05 V in the embodiment)." See Utsunomiya et al. col. 7, lines 60-63. Within a reasonable process variation, the threshold voltages of these transistors could easily be 0 V or slightly less than 0.

In Figure 10 of Utsunomiya et al., M0 is the first stage MOSFET. With a threshold voltage of less than 0 V, the boosting circuit of Figure 10 would fail to pump up the output voltage Vpp, because reverse current flow through M0 would prevent charge accumulation at the source of M0.

On the other hand, amended claim 1 recites a native transistor in the first stage of the charge pump with a threshold voltage that is greater than zero over a voltage range caused by

process variations. Process variations typically cause variations of less than 0.1 volts in the threshold voltage of a FET. The present application discloses that the native FET has a threshold voltage of, for example, 0.3 volts. See the present application at, e.g., page 6, lines 12-14. Therefore, the native transistor of amended claim 1 remains above zero despite process variations.

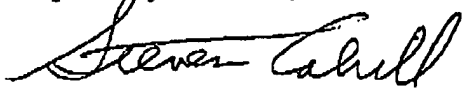
For these reasons, amended claim 1 is novel and nonobvious over the cited prior art. Claim 12 is novel and nonobvious over the cited prior art for similar reasons.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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